WHAT IS CLAIMED IS:

1. A computer program product, encoded in computer readable media, the computer program product for designing an integrated circuit chip, comprising:

a first set of instructions, executable on a computer system, the first set of instructions configured to model an input/output cell located on the perimeter of an integrated circuit, the model of the input/output cell further comprising:

a model of a main cell; and

a model of a pre-cell; and

a second set of instructions, executable on a computer system, the second set of instructions configured to model a cover wherein the cover prevents an area occupied by the pre-cell from being used for any other purpose in the model.

2. The computer program product as recited in claim 1, further comprising:

a third set of instructions, executable on a computer system, the third set of instructions configured to adjust the timing of the main-cell and pre-cell, wherein the timing adjustment to the main cell and pre-cell approximates the timing of a input/output cell.

3. The computer program product as recited in claim 1, wherein the first cover is used to cover a first pre-cell, further comprising:

a second pre-cell, wherein a single input/out put cell is modeled with a main-cell, a first pre-cell and a second pre-cell, wherein the first cover prevents use of the area of the first pre-cell and the second cover prevents use of the area covered by the second pre-cell.

4. The computer program product as recited in claim 1, the computer program product further comprising:

a database, wherein the database stores a netlist.

5. The computer program product as recited in claim 1, the computer program product further comprising:

a third set of instructions, the third set of instructions configured to convert a netlist to a proprietary format.

6. The computer program product as recited in claim 1, further comprising:

a third set of instructions, the third set of instructions configured to flatten a netlist by reading a description of the function of a cell and listing each function of the cell individually, wherein reading a description of the function of a cell and listing each function of the cell individually.

7. The computer program product as recited in claim 1, further comprising:

a third set of instructions, the set of instructions configured to identify the location of each pin in an integrated circuit.

8. The computer program product as recited in claim 1, further comprising:

a third set of instructions, the third set of instructions configured to identify the location of each cell in an integrated circuit.

9. A method of designing an integrated circuit, the method to model an input/output cell in a location on the perimeter of the integrated circuit and a location in the core area of the integrated circuit, the method comprising:

modeling an input/output cell located on the perimeter of an integrated circuit, wherein modeling the input/output cell further comprises:

modeling a main cell; and

modeling a pre-cell; and

modeling a cover wherein the cover prevents an area designated to occupied by the model of the pre-cell from being used for any other purpose in the model.

10. An integrated circuit manufactured by the method as recited in claim 9.

11. The method as recited in claim 9, further comprising:
adjusting the timing of the main-cell and pre-cell, adjusting the timing of the main cell and the pre-cell approximates the timing of a input/output cell.

12. The method as recited in claim 9, further comprising:
modeling the input/out put cell with a main-cell, a first pre-cell and a second pre-cell, wherein the first cover prevents use of the area of the first pre-cell and the second cover prevents use of the area covered by the second pre-cell.

13. The method as recited in claim 9, further comprising:
storing a netlist.

14. The method as recited in claim 9, further comprising:
converting a netlist to a proprietary format.

15. The method as recited in claim 9, further comprising:
listing each function of a cell individually.

16. The method as recited in claim 9, further comprising:
identifying the location of each pin in an integrated circuit.

17. The method as recited in claim 9, further comprising:
identifying the location of each cell in an integrated circuit.

18. A computer system, comprising:
a memory; and
a central processing unit, wherein the central processing unit is designed with the assistance of a computer program, the computer program encoded in computer readable media, the computer program product comprising:

a first set of instructions, stored in said memory, configured to model an input/output cell located on the perimeter of an integrated circuit; the model of the input/output cell further comprising:

a model of a main cell; and

a model of a first pre-cell; and

a second set of instructions, stored in the memory, configured to model a cover wherein the cover prevents the area occupied by the first pre-cell from being used for any other purpose in the model.

19. The computer system as recited in claim 18, further comprising:

a third set of instructions, executable on a computer system configured to adjust the timing of the main-cell and pre-cell, wherein the timing adjustment to the main cell and first pre-cell approximates the timing of a input/output cell.

20. The computer system as recited in claim 18, further comprising:

a third set of instructions, executable on a computer system configured to:

model a second pre-cell and model a second cover, wherein the first cover prevents use of the area of the first pre-cell and the second cover prevents use of the area covered by the second pre-cell.

21. The computer system as recited in claim 18, further comprising:

a database, wherein the database stores a netlist.

22. The computer system as recited in claim 18, further comprising:

a third set of instructions, the third set of instructions configured to convert a netlist to a proprietary format.

23. The computer system as recited in claim 18, further comprising:

a third set of instructions, the third set of instructions configured to read a description of the function of a cell and list each function of the cell individually, wherein reading a description of the function of a cell and listing each function of the cell individually is referred to as flattening a netlist.